poly-germanium can later be reacted with a germanide forming metal such as nickel. Additionally, any poly-SiGe alloy can also be used to substitute poly-Si **113**. Still further, poly-Si **113** can be deposited in a poly-crystalline form or deposited in an amorphous form which is later transformed into poly-Si when exposed to high temperature.

With reference to FIGS. **5** and **6**, a metal **116**, such as nickel (Ni), platinum (Pt), cobalt (Co), tungsten (W) and/or titanium (Ti), for use in silicide formation is then blanket deposited over the device. The metal **116** covers horizontal surfaces and inner and outer sidewalls of the poly-Si **113**. The metal **116** is annealed and, once annealed, reacts with the poly-Si **113** to form a silicide **120**, as shown in FIG. **6**. In the present embodiment, the "FUSI first" silicide **120** formation propagates generally sideways and, for particularly short FUSI gates, such as gates that are **50** nm or less in length, this sideways directed silicide **120** formation enables the deposition of relatively thin metal layers since the reaction takes place from both gate sidewalls. The formation of silicide **120** by sidewall reaction is, in some cases, more beneficial than the conversion of the poly-Si **113** gate to silicide by reacting the silicide forming metal **116** from the top surface of the poly-Si **113** gate downward.

The choice of silicide **120** is at least partially made to induce radial strain and, optionally, longitudinal strain in the reshaped nanowire **108** channel and is generally free of other considerations related to threshold voltage tuning since it is the thin gate conductor **117** and not the silicide **120** that sets the gate conductor work function. Additionally, since dopant incorporation for source/drain formation is carried out later in the process flow the choice of the silicide **120** to be employed is not limited by the silicide **120** formation temperature. For example, $TiSi_2$, which forms at about 750° C., can be used. Following the silicide **120** formation, unreacted metal **116** may be selectively etched with respect to the silicide **120** and the dielectric surfaces (e.g. **112**, **102** and **115**).

With reference now to FIGS. **7-9**, if the exposed TaN film **117** was not removed during the gate etch as described in the embodiment of FIGS. **4**C and **4**D, it is now selectively etched with respect to the silicide **120** and the gate dielectric **112**. Gate sidewall spacers **121** are then formed and epitaxy **122** may be selectively used to thicken the reshaped nanowire **108** portions that are not encapsulated by the gate stack **118** and sidewall spaces. The SOI pads **103**A may also be thickened as necessary by epitaxy **122**. Epitaxy **122** can include in-situ doping to incorporate dopants into the source/drain regions. Alternatively, ion-implantation can be used to dope the source and drain region. As shown in FIG. **9**, self-aligned silicide is applied to form silicide **124** over the source and drain.

In accordance with further embodiments, the methods disclosed herein can be applied to an omega-shaped gate nanowire FET, where the nanowire **104**/reshaped nanowire **108** is attached to the buried oxide **102** such that it is not suspended. In this non-suspended case, however, the strain profile may not have perfect radial symmetry. Volume expansion plays a smaller role in producing stress in the silicided films, and it is assumed that thermal mismatch between the silicide **120** and the nanowire **104**/reshaped nanowire **108** is a main contributor to stress. As such, an intensity of the induced strain can be controlled and tuned by changes in the silicide formation temperature. In general, the higher the formation temperature, the higher the induced strain due to thermal mismatch.

The above embodiments describe a method and structure to induce radial strain in a nanowire FET channel. The radial strain can be decoupled from the longitudinal strain. The choice of stressor (FUSI) does not change the gate stack properties (work function).

While the disclosure has been described with reference to exemplary embodiments, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted for elements thereof without departing from the scope of the disclosure. In addition, many modifications may be made to adapt a particular situation or material to the teachings of the disclosure without departing from the essential scope thereof. Therefore, it is intended that the disclosure not be limited to the particular exemplary embodiment disclosed as the best mode contemplated for carrying out this disclosure, but that the disclosure will include all embodiments falling within the scope of the appended claims.

What is claimed is:

1. An intermediate process device, comprising:
- a nanowire connecting first and second silicon-on-insulator (SOI) pads;
- a gate including a gate conductor surrounding an entire length of the nanowire and poly-Si surrounding the gate conductor, the entire length of the nanowire being defined as all upper, lower and side surfaces of the nanowire along the length of the nanowire; and
- silicide forming metal disposed to react with the poly-Si to form a fully silicided (FUSI) material to induce radial strain in the nanowire.

2. The device according to claim **1**, wherein a material of the gate conductor is selected from the group comprising tantalum nitride (TaN) and titanium nitride (TiN).

3. The device according to claim **1**, wherein the gate conductor comprises a film having a thickness of about 2-4 nm.

4. The device according to claim **1**, wherein the fully silicided material comprises a silicide that forms above about 550° C.

5. The device according to claim **1**, wherein the fully silicided material comprises at least one of nickel (Ni), platinum (Pt), cobalt (Co), tungsten (W) and titanium (Ti).

6. The device according to claim **1**, wherein a material of the gate conductor is determinative of a work function of the gate conductor independent of the fully silicided material.

7. An intermediate process device, comprising:
- first and second pads;
- a nanowire, formed in a silicon-on-insulator (SOI) layer disposed over a buried oxide (BOX) layer, connecting the first and second pads;
- a gate surrounding an entire length of the nanowire and including a dielectric adjacent the nanowire, a gate conductor adjacent the dielectric and poly-Si surrounding the gate conductor, the entire length of the nanowire being defined as all upper, lower and side surfaces of the nanowire along the length of the nanowire; and
- silicide forming metal disposed at least along sidewalls of the poly-Si to react with the poly-Si to form a fully silicided (FUSI) material to induce radial strain on the nanowire.

8. The device according to claim **7**, wherein the nanowire is substantially cylindrical.

9. The device according to claim **7**, wherein the gate perimetrically surrounds the nanowire.

10. The device according to claim **7**, wherein a material of the dielectric is selected from the group comprising silicon dioxide (SiO_2), silicon oxynitride (SiON) and hafnium oxide (HfO_2).